REMARKS

In the previous office action, Claims 1-10 were examined and rejected. Claims 1 and 3 are amended; no claims are added; no claims are canceled. Applicant asserts that no new matter is added herein as the amendments to Claims 1 and 3 are supported at paragraphs 21 and 24-26; and **Figures 3-4, 6, 9**, and **12-13** of the application as originally filed. Applicant respectfully requests reconsideration of Claims 1-10, as amended, in view of at least in the following.

I. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejects Claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,696,732 to Matsuoka, et al. ("Matsuoka") and U.S. Patent No. 5,541,427 to Chappell, et al. ("Chappell"). To render a claim obvious, all elements of that claim must be taught or suggested by at least one properly combined reference.

Applicant respectfully disagrees with the rejection above and submits that independent Claim 1 is allowable for at least the reason that the cited references do teach or suggest a contact extending a first depth through a first thickness of a dielectric layer to a gate, and extending a different second depth through a portion of a second thickness greater than the first thickness, short of the junction region as required by Claim 1. According to Claim 1, for example, a contact may extend through a first thickness of a dielectric to contact a gate, and extend deeper into a second thickness of the dielectric over a junction region adjacent to the gate short of the junction region (e.g., **Figures 3-4** and **12-13**). Similarly, the contact may extend into the thicker

thickness of dielectric adjacent to the gate, to a lesser depth than the first thickness (e.g., see **Figures 6** and **9**).

Matsuoka describes gated device 14c in an SRAM cell having first and fourth contacts 44, 46 which either go through the dielectric layer and either stop at the etch stops or go to the gate, or a junction region 14a, b (see **Figure 23** and col. 10, lines 9-35). First to fourth contacts 44 and 46, each extend only through one thickness of the dielectric.

In addition, Matsuoka describes local wiring 24 connecting gate electrode 14c to source/drain region 14b, as well as to source/drain region 16a (See Figure 2 and col. 6, lines 52-61). However, Matsuoka does not teach or suggest a contact extending a first depth through a first thickness to the gate, and a different second step through a portion of the second thickness, short of the junction region adjacent the gate, as required by amended claim 1.

Chappell describes dielectric layers 32 and 34 above gate 18 and over at junction region 31 adjacent to the gate (See **Figures 3-5** and col. 4, lines 13-28). Moreover, Chappell describes that layer 32 is a bilayer having a lower conformal coating of the silicon dioxide followed by an upper conformal coating of aluminum oxide so that when the aluminum oxide is stripped, the silicon dioxide acts as a buffer to protect the underlying diffusion (e.g., region 31) (See col. 4, lines 14-20). Specifically, as shown in **Figure 5**, opening 40 extends to a similar depth in the dielectric (col. 4, lines 29-37). Thus, opening 40 does not teach or suggest the different second depth limitation of Claim 1.

Similarly, opening 42 is borderless to the gate and does not contact electrically conductive portions of the gate (See col. 4, lines 38-48). Hence, opening 42 does not teach or suggest the extending to the gate limitation of Claim 1. Hence, since neither Matsuoka, Chappell, nor the combination teaches or suggests the contact as claimed in amended Claim 1, Applicant respectfully requests that the Patent Office withdraw the rejection above for independent Claim 1.

Applicant submits that dependent claims 2-10, being dependent upon allowable base Claim 1, are patentable over the cited reference for at least the reasons explained above. Thus, Applicant respectfully requests that the Patent Office withdraw the rejection of dependent claims 2-10 noted above.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance, and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 6/2/05

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on June 7, 2005.

Lillian E. Rodriguez 6-7-05

Lillian E. Rodriguez June 7, 2005